A MIXED-MODE ARTIFICIAL NEURAL NETWORK MODEL APPLIED TO SENSOR OUTPUT IMPROVEMENT

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ABSTRACT: This paper explains the design and simulation of an artificial neuron using a current-mode mixed signal four-quadrant multiplier and a class AB non-linear output function as arithmetic building blocks. The proposed neuron model has been used to simulate a small sensor linearization system, applied to the improvement of negative temperature coefficient resistor output. System simulation results and application performance applied to four different temperature sensor samples are presented.

INTRODUCTION

Artificial Neural Networks (ANNs) are computing tools based on the mammalian nervous system operation. Basically it consists of several (sometimes many) small processing elements, called artificial neurons, highly interconnected and arranged in layers. The input-output function carried out by these systems is learned by means of a training process where input-output data pairs are iteratively presented, adjusting the system free parameters (called weights) that connect inputs from a neuron layer with the preceding neuron layer outputs. ANNs can be implemented in several ways, depending on the application requirements. Thus, in systems where size, power consumption and speed are main requirements, electronic analog implementation is a suitable selection [1]. Today, shrink bias voltages makes difficult to processing data in voltage-mode. In this case, current-mode processing gives better results at lower bias, reducing the power consumption [2].

On the other hand, implementation of reliable long-term and mid-term analog programmable weights results very hard due to mismatching and offsets. Due to the high accuracy of digital storing data for long and mid-term in register-based structures, the combination of both electronic technologies can improve the system features. Previous works [3] have presented the use of mixed-mode multipliers in artificial neuron implementation, showing promising results applied to real problems.

This paper presents the analysis and simulation of a current-mode based artificial neural network with digital weight storage and its application to a real problem, the linearization of a negative temperature coefficient resistor.

The paper is structured as follows: In the next section design and architecture of a current-mode mixed analog-digital artificial neuron is presented. Afterwards simulation results of this processing element behaviour implemented in AMS 0.35µm technology are shown. Following we study the use of this processing block implementing on a Multilayer Perceptron Network (MLP) applied to a real application, the improvement of a temperature sensor output, giving results for four different sensor samples. Finally, some conclusions and future work are proposed.

PROCESSING ELEMENT IMPLEMENTATION

The proposed artificial neuron has been implemented using the Austria Microsystems (AMS) 0.35µm design kit. Maximum processing currents are limited to ± 50 µA, voltage bias are limited to 3.3v in the inverters and ±2v in the rest of the multiplier structure.

Mixed Digital-Analog Four-Quadrant Multiplier

The proposed multiplier block contains a class AB current follower (Fig. 1) controlled by the sign bit of the digital operand plus a 7-bit digitally programmable current divider (Fig. 2). Current output ranges from I_{in} to $-I_{in}$. An analog multiplexer selects the analog operand input path to the digital current divider. When the weight sign bit is positive (b_0=0v), current goes to the

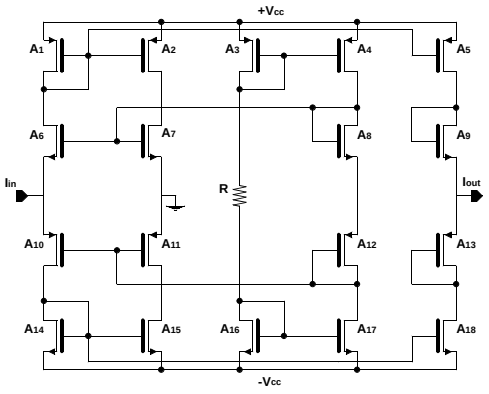

Fig. 1. Class AB current follower

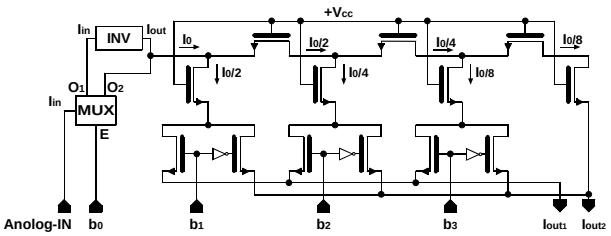

Fig. 2. Only three–bits four quadrant mixed analog-digital multiplier (ADM)

divider straight; if sign bit is negative (b0=3.3v), current is driven to the current follower, changing the sign of the output current.

Programmable Current Divider. The main four-quadrant multiplier building block consists of an R-2R ladder structure [4] implemented with NMOS transistors. This structure (Fig. 2), widely presented in the literature [5], [6], [7], allows the current to flow in both directions and is designed using identical 0.3µm length and 10µm width transistors working in triode mode.

Gate voltages b_i (Fig. 2) control the current flow to the right-side transistors (b_i=0v) or the left-side transistor (b_i=3.3v). For N bits, output current is described according to

$$I_{out_1} = I_0\left(\frac{1}{2^N} + \sum_{n=1}^{N}\frac{\bar{b}_n}{2^n}\right) \quad (1)$$

$$I_{out_2} = I_0\left(\sum_{n=1}^{N}\frac{b_n}{2^n}\right) \quad (2)$$

where I_{out1} and I_{out2} are the lower and upper output currents. In our work, I_{out2} has been selected as the final output current. Thus, according to (1), digital weight absolute value ranges from 0 to $1-1/2^N$. Assuming a 7 bits plus sign weight representation, digital operand minimum module value equals to $7.8125\cdot10^{-3}$.

Current Follower. Multiplier sign bit is implemented using a class AB current follower scheme presented on [8] (Fig. 1). This structure gives a centred low-distortion current using a ± 2v bias voltage. Tables 1 and 2 show the current follower design characteristics and transistor sizes, respectively. The bias current value (30µA, see Table 1) ensures a very low distortion in the processing signals range [9]. The resistor value in the middle of the structure is 66.66kΩ.

Activation Function

Activation function circuit consists of a class AB current conveyor (Fig. 3), similar to the circuit proposed in [10]. Circuit output has a *tanh* type behaviour. Design characteristics and transistor dimensions are shown in Tables 3 and 4 respectively.

TABLE 1. Current follower design characteristics

$\pm V_{cc}$ [V]	±2
I_{bias} [µA]	30
Vgs [V]	±1
Vds [V]	±1

TABLE 2. Current follower transistors dimensions

Transistors	W [µm]	L [µm]
A_1,A_2,A_3,A_4,A_5	4.25	0.3
A_6,A_7,A_8,A_9	13.00	0.3
A_{10},A_{11},A_{12},A_{13}	48.15	0.3
A_{14},A_{15},A_{16},A_{17},A_{18}	0.85	0.3

TABLE 3. Activation function design characteristics

$\pm V_{cc}$ [V]	±2
I_a [µA]	5
I_b [µA]	50
V_{gs} [V]	±1
V_{ds} [V]	±1

TABLE 4. Activation function transistors dimensions

Transistors	W [µm]	L [µm]
B_1, B_2, B_3	0.9	0.3
B_4	5.35	0.3
B_5, B_6, B_7	6.9	0.3
B_8, B_9	1.9	0.3
B_{10}	2.85	0.3
B_{11}	0.65	0.3
B_{12}, B_{13}	8.7	0.3
B_{14}	0.7	0.3
B_{15}	0.6	2.1
B_{16}, B_{17}, B_{18}	0.6	1.7
B_{19}	1.2	0.3
B_{20}, B_{21}, B_{22}	1.4	0.3

CIRCUIT SIMULATION

Artificial neuron circuit simulation was carried out using two different simulators (Spectre and Hspice) using Cadence Design Framework, obtaining similar results.

Mixed Digital-Analog Four-Quadrant Multiplier

Table 5 show results of the current follower simulation. As can be seen, the circuit shows a 5% loss current (slope is not 1) that can be reduced replacing the simple current mirrors used in the design with cascode current mirrors. On the other hand, offset effects are very low.

The mixed-mode multiplier behaviour has been numerically modelled using Matlab. Real multiplier operation is expressed by:

$$out = 0.974865wp - 0.0136726p \quad (3)$$

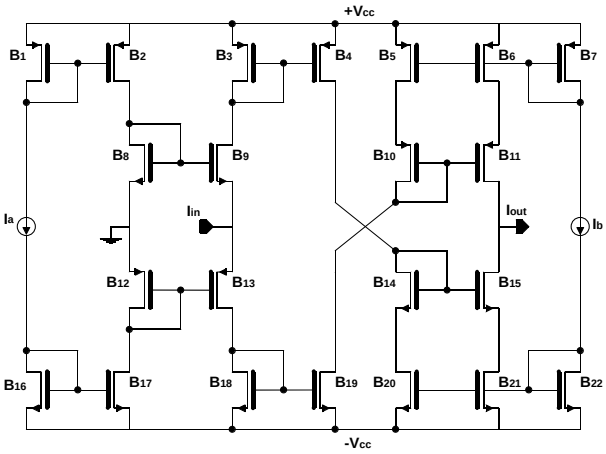

Fig. 3. Class AB activation function

TABLE 5. Current follower: Simulation results

I_{off} [nA]	0.74
V_{off} [µV]	65
Slope	0.951166

Where *w* is the digital weight and *p* is the analog current input to the analog-digital multiplier. Results are shown in Fig. 4. Fig. 5 presents the differences between the ideal operation and the real operation of the multiplier.

Non-Linear Activation Function

Non-linear output function has been modelled using a 1-15-1 MLP. Simulation model and ideal *tanh* output functions are shown in Fig. 6. Differences between simulated circuit and ideal output are presented in Figure 7.

REAL APPLICATION EXAMPLE: SENSOR LINEARIZATION

The following example has been widely analyzed in the literature [11], [12], [13]. It consists in conditioning the response of a nonlinear sensor with sigmoid output using a MLP. There are diverse sensors with this output characteristic form (such as giant magnetoresistive sensors [14]). In this work, we have used the well-characterized negative temperature coefficient resistor (NTC) connected on a resistive divider, which voltage output is shown in Fig. 8. In this case, the MLP output provides the correction that must be added to the sensor characteristic to linearize the total behaviour.

In order to verify that results are independent of the sample we used four datasets from four different NTC sensors, training the network for each one of them.

Patterns of each NTC consist of 71 sensor output voltages collected in the 253-323K temperature range.

For each NTC, data are divided in two datasets, consisting of 61 patterns for the learning process and 10 patterns for the verification phase. These validation patterns are randomly selected from the whole dataset.

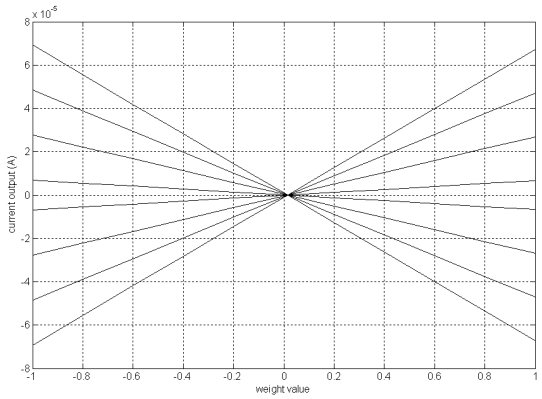

Fig. 4. Mixed-mode four-quadrant multiplier output

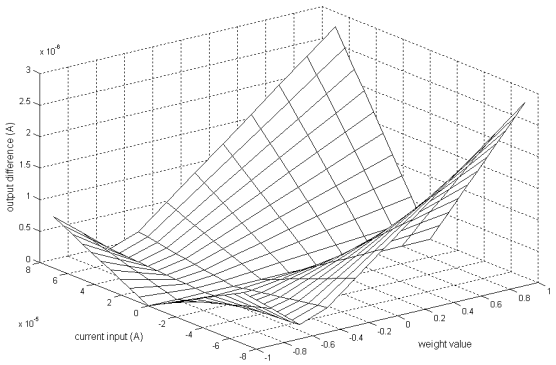

Fig. 5 Differences between the ideal and simulated mixed-mode multiplier

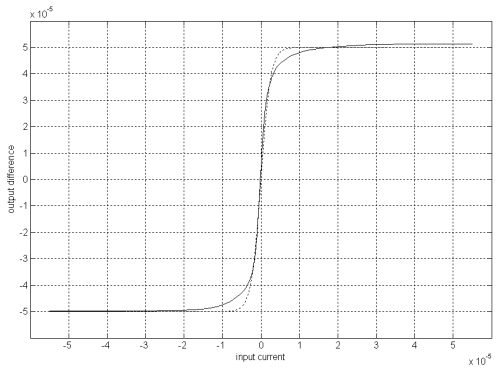

Fig. 6. Non-linear output function: Ideal (dotted line) and real (continuous line)

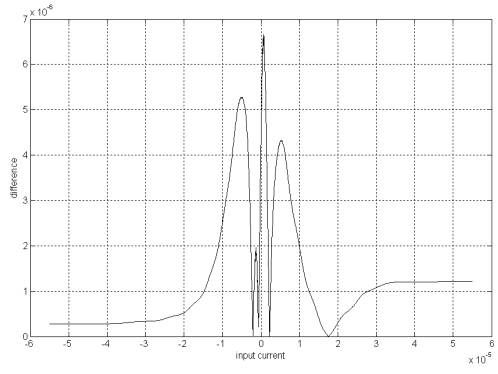

Fig. 7.Differences between the real and ideal operation of the activation function

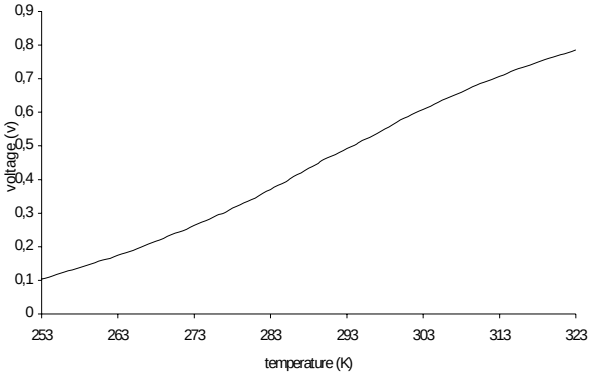

Fig. 8. NTC output voltage (connected on a resistive divider).

Network Architecture

Previous works [3] show that a 1-1-3-1 MLP network architecture gives the best performance results in this case. The used neural network scheme is shown in Figure 9. Output function of the first hidden and output layer neurons are linear, while the neurons in the second hidden layer have the *tanh* designed circuit as output function. All of them use the analog-digital multiplier designed and explained before. The use of the real multiplier model and non-ideal activation function makes necessary to double the number of hidden neurons, compared to the use of ideal elements in the neuron definition. On the other hand, accuracy in digital weights must be carefully selected. Considering circuit size restrictions and minimum accuracy, an 8-bit representation of the weights (with positive and negative codification) gives a good system performance.

Training Results

The resulting artificial neural network is trained on a computer. Our experience confirms that learning algorithms based on error back-propagation have demonstrated a worse efficacy in network weight adaptation in systems with high non-linearities and offsets, compared to perturbative techniques [15], [16]. These methods evaluate output error variations due to small random weight changes. If a random variation makes the error to decrease, the weight change is accepted; otherwise, weight remains unchanged. This methodology is not dependent on the arithmetic operations carried out by the artificial neuron. However, in standard back-propagation algorithms the use of different arithmetic operations can change drastically the network learning behaviour.

Although there are proposed in the literature several parallel perturbative algorithms developed for systems with digital weight storage [17], the learning algorithm applied in this work is based on the classical serial weight-perturbation algorithm presented in [18].

Fig. 10 shows the corrected output voltage compared to the ideal expected output (dashed line) after 8-bit resolution weight discretization. As this figure shows, the output error remains lesser than 1K between 250K and 310K.

The ANN generalization ability is analyzed using the validation dataset and the corresponding network output. In all four examples, output error keeps lower than 1K in the same range from 250K to 310K (Figure 11).

CONCLUSIONS AND FUTURE WORK

In this paper a class AB current-mode mixed analog-digital processing element designed for implementation of artificial neural networks is presented. The system consists of a four-quadrant mixed analog-digital circuit that multiplies the analog input current by an 8-bit digital weight. The multiplier output is processed by a class AB current-mode non-linear circuit that gives the final neuron output.

This circuit has been designed using the 0.35μm AMS technology. Simulation results have been used to developing a numerical model of the neuron, including it in a MLP network model. In order to validate the use of these circuits in real-world applications, the MLP has been applied to correct the non-linearity of four different negative coefficient temperature sensors. Results show an application range extension (error lower than 1 degree) of 50% or more.

The next goal is to reduce the output error drift at the

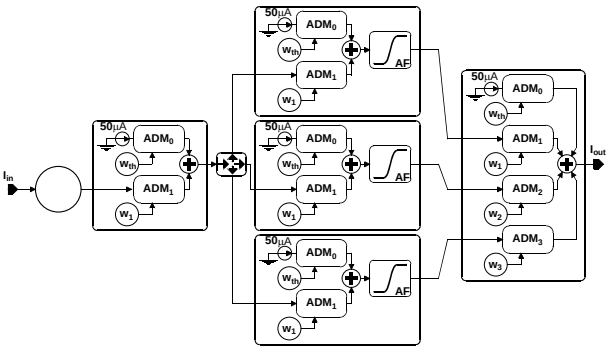

Fig. 9. MLP architecture

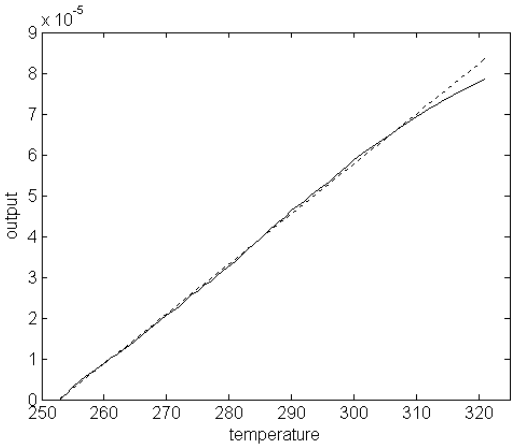

Fig. 10. Corrected output voltage versus ideal linear output

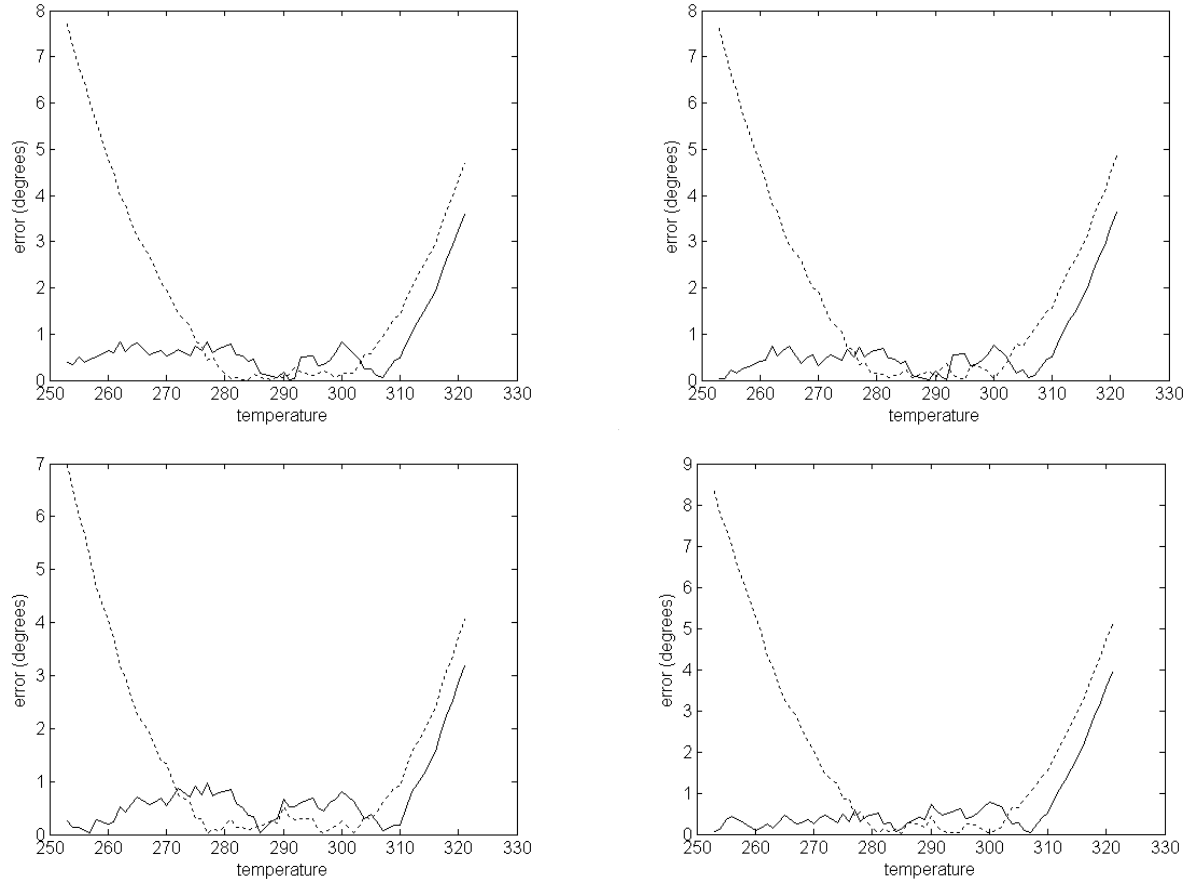

Fig. 11. NTC output error compared to neural network output error for four different NTC sensors

end of the sensor span (from 310K to 325K), modifying the design in order to minimize the effects of mismatching and offsets.

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